

JAIRO RODRIGO MEJIA APONTE

Embedded Software Developer

@ jairo.mejia.2708@gmail.com
in linkedin.com/in/jairo-mejia/

☎ (+49) 1516 480 6126
🔗 github.com/jrmejiaa/

📍 Frankfurt am Main, Germany



EXPERIENCE

Embedded Software Linux Developer

Belden Inc.

📅 Since July 2023

📍 Frankfurt, Germany

Promoted from Junior in 18 months for outstanding performance. Developing embedded C++ software for next-generation wireless industrial routers (4G/5G, WiFi, GPS) targeting rail, autonomous driving, and fleet geolocation on a Yocto-based Linux platform.

- Co-designed and own the ModemManager D-Bus client in C++, managing cellular modem lifecycle and configuration via AT commands and QMI protocol on a Yocto-based Linux platform.
- Built an end-to-end whitebox testing framework based on Yocto's ptest strategy, validating the full communication path from NETCONF frontend through ZMQ to D-Bus backend on both QEMU and real hardware.
- Contributed to WiFi (AP, mesh, driver-level) and GPS (time synchronization, geolocation) subsystems.
- Mentored team during legacy product handoff.

M.Sc-Thesis: Design and test a configurable cache system

ESA Group - Technische Universität Darmstadt

📅 November 2022 – July 2023

📍 Darmstadt, Germany

Implement and attach a configurable cache hierarchy to a RISC-V core using the Bluespec compiler to create the needed HDL code. Later on implement a verification tool based on Python for the HW design with QUESTA and cocotb. Finally, verify the implementation running some benchmarks and desired software in the implemented multi-core.

Researcher Engineer on 4G/5G cores for Open Networks

NTT Data

📅 February 2020 – April 2021

📍 Bogotá, Colombia

Analysis, investigation, and development of Cloud-Native Linux-based software tools to integrate different open-source 5G and 4G cores with and without compliant 3GPP protocols.

Intern on R&D Department of RF Systems

National Instruments

📅 April 2018 – January - 2019

📍 Dresden, Germany

Implementation of a digital control based on a SPI protocol using VHDL and LABVIEW FPGA Programming to make the communication between a 4G RF SDR Device and external hardware. Finally, measure and verify the integrity of the created signal (Speed rate, input/output impedance) of the interface.

HARD SKILLS

C/C++ Bash Python Yocto
cmake/make VHDL Verilog
Bluespec Git MySQL/SQL
Openstack k8s RISC-V Core
ARM Core Systems STM32 HAL

LaTeX Microsoft 365 Windows
Linux G Suite Management Apps

SOFT SKILLS

Social skills Public speaking
Visual and Verbal communication

Adaptability Critical thinking
Desire to learn Innovation

Decision-making Project management
Inspiring people Enthusiasm

Collaboration Diversity awareness
Intercultural competence Empathy

LANGUAGE SKILLS

Spanish ●●●●●

English ●●●●●

German ●●●●●

PROUD OF

🎓 Scholarship holder of FES for my Master
Since 01. January 2021

✈ Exchange program in Germany
Oct 2017 – Jan 2019

🏛 One of the best graduates in my year
November 2019

EDUCATION BACKGROUND

M.Sc. Informationssystemtechnik

Technische Universität Darmstadt

📅 Since November 2020

B.Sc. Electronic Engineering

Universidad Nacional de Colombia

📅 February 2013 – November 2019

Exchange year. Elektrotechnik und Informationstechnik

Technische Universität Ilmenau - Germany

📅 October 2017 – January 2019

REFERENCIAS

Jürgen Henke

📍 Belden Inc.

@ jurgen.henke@belden.com

Volkan Öz

📍 National Instruments Dresden

@ volkan.oez@ni.com

Olaf Arendt

📍 National Instruments Dresden

@ olaf.arendt@ni.com

Prof. Jan Bacca Rodriguez

📍 Universidad Nacional de Colombia

@ jbaccar@unal.edu.co